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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,263	10/21/2003	Dominik J. Schmidt		4606

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,263	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *11-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 4/14/2006 AU2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 10 have been examined.

Election/Restrictions

2. Newly submitted claims 11 – 20 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Newly submitted independent claim 11 is directed to a combination claim. Newly submitted independent claim 17 is directed to a mode selection and coupling method. Both of the independent claims would have been restricted in the first office action if they had been presented when prosecution had begun.

FWS 4/14/2006

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 11 – 20 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Arguments

3. Applicant's arguments filed on 09 February 2006 have been fully considered but they are not persuasive.

As per Applicants argument of the 35 U.S.C. § 102(b) rejection of independent claim 1, Applicant argues that the relied upon reference, US Patent No. 5,793,989 (hereinafter Moss), does not teach a common set of pins coupled to the first and second

interface circuits and a host computer bus, or that the common set of pins are user selectable to communicate with the host computer bus in accordance with either a first or second bus standard. Examiner submits that Moss does teach all of the limitations of amended claim 1. Moss teaches a common set of pins (Figure 1 Item 105) coupled to the first and second interface circuits (Figure 1 Items 112 and 113) and a host computer bus (Figure 1 Item 127). Moss also teaches that the common set of pins are user selectable to communicate with the host computer bus in accordance with either a first or second bus standard because the user ultimately in the end selects the pin format. Socket Logic Unit (Figure 1 Item 109) represents the "user selectable" function because it selects the mode of common set of pins (Figure 1 Item 105).

As per Applicants arguments of the 35 U.S.C. § 103(a) rejection of claims 7 and 8, Applicant argues that the relied upon reference, US Patent No. 5,793,989 (hereinafter Moss), does not teach an interface circuit that formats signals on an internal bus that is coupled to both interface circuits. Applicant argues that in Moss, dedicated busses exist (Figure 1 Items 114, 115, 116, and 119), each of which provides signals on only a single standard to the interface circuits. Examiner submits that the signals on the internal busses (Figure 1 Item 115 and 119) are formatted by the interface circuits (Figure 1 Items 112 and 113) to a format that is appropriate to be sent on the internal radio busses (Figure 1 Items 114 and 116).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 2, and 4 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Moss et al. US Patent No. 5,793,989 (hereinafter Moss).

As per claim 1, Moss teaches a first interface circuit conforming to a first bus standard (Figure 1 Item 113); a second interface circuit conforming to a second bus standard (Figure 1 Item 112); and a common set of pins (Figure 1 Item 105) coupled to the first interface circuit and the second interface circuit and a host computer bus (Figure 1 Item 127), the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard. The bus standard that is used to send data through the pins is selected by Mode Selecting Means (Figure 2 Item 201) and is controlled by setting a code signal on the address or control lines (Col 3 Line 65 – Col 4 Lines 1, and Col 4 Lines 17 – 27).

As per claim 2, Moss also teaches wherein the common set of pins (Figure 1 Item 105) conforms to the Personal Computer Memory Card International Association (PCMCIA) bus standard (Col 2 Lines 32 – 38).

As per claim 4, Moss also teaches wherein the second bus standard is the PCMCIA bus standard (Figure 1 Item 112, Col 2 Lines 32 – 38).

As per claim 5, Moss also teaches the pins of the connector are connected to a multi-voltage buffer (Col 45 Lines 45 – 53 [tristate buffers]).

As per Claim 6, the first and second circuits are connected to internal busses (Figure 1 Items 114, 115, 116, and 119, Col 2 Lines 32 – 38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moss et al. US Patent No. 5,793,989 (hereinafter Moss) in view of Tyson "How PCI Works" (hereinafter Tyson).

As per claim 3, Moss teaches a system that allows for the dual function of a peripheral card as described per claim 1 above.

Moss does not teach that one of the bus standards is the Peripheral Component Interconnect (PCI) bus standard.

Tyson teaches that computers use the PCI bus standard to connect to peripherals (Tyson; Page 4 Paragraph 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the PCI bus standard in the system of Moss et al. Using the PCI bus standard in a peripheral allows for utilization of Plug-and-Play (PnP) with the device (Tyson; Pages 5 – 6 [Plug and Play]).

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moss et al. US Patent No. 5,793,989 (hereinafter Moss).

As per claims 7 and 8, Moss teaches a system that allows for the dual function of a peripheral card as described per claim 6 above.

Moss does not explicitly teach that the first or second interface circuits format signals on the internal busses to be compliant with the first or second bus standard.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the interface units of Moss interpret the signals on the internal busses and formats them into signals compliant with appropriate bus standard because in order to communicate with the radio unit (Figure 1 Item 117), the interface circuits must format data between their respective standard and the standard used by the radio busses (Figure 1 Items 114 and 116) that connect to the radio unit.

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moss et al. US Patent No. 5,793,989 (hereinafter Moss) in view of Cahill et al. US Patent No. 6,871,244 (hereinafter Cahill).

As per claims 9 and 10, Moss teaches the system that allows for the dual function of a peripheral card as described per claim 1 above.

Moss does not teach where the system comprises a first or second power supply to supply voltage swings in accordance with the first or second bus standard.

Cahill teaches a system of selecting a bus standard to use similar to that of Moss. Cahill also teach where in the selection, a power conversion is performed when needed by a power supply to convert signal voltages to those appropriate for the bus standard (Cahill; Figure 3 Items 162 and 166, Col 6 Lines 20 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the power supply of Cahill et al. in the system of Moss et al. to supply voltages that are compliant with the appropriate bus standard (Cahill et al.; Col 6 Lines 29 – 33).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jolley et al. US Patent No. 5,832,244 (hereinafter Jolley) teaches many limitations of the claimed invention. Jolley teaches a first interface circuit (Figure 1 Item 26) conforming to a first bus standard; a second interface circuit (Figure 1 Item 28)

conforming to a second bus standard; and a common set of pins (Figure 1 Item 20) coupled to the first interface circuit and the second interface circuit and a host computer bus (Figure 1 Item 18), the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard (Col 4 Line 62 – Col 5 Line 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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4/14/2006